WHAT IS CLAIMED IS:

1. A plurality of metal bumps for connecting a nonconducting substrate and a chip, comprising:

at least a first metal bump having a first sidewall, the first sidewall comprising a first predetermined area; and

at least a second metal bump having a second sidewall, the second sidewall comprising a second predetermined area adjacent to the first predetermined area;

wherein at least the first predetermined area is covered with an insulating layer.

2. The plurality of metal bumps of claim 1, wherein the second predetermined area is covered with an insulating layer.

3. The plurality of metal bumps of claim 1, wherein the second sidewall further comprises a third predetermined area outside the second predetermined area, and the third predetermined area is covered with an insulating layer.

4. The plurality of metal bumps of claim 1, wherein the first sidewall is completely covered with an insulating layer.

5. The plurality of metal bumps of claim 1, wherein the first sidewall and the second sidewall are both completely covered with an insulating layer.

6. The plurality of metal bumps of claim 1, wherein the nonconducting substrate comprises a plurality of first metal pads, and the chip comprises a plurality of second metal pads which correspond to the first metal pads.

7. The plurality of metal bumps of claim 6, wherein each metal bump is fixed between the first metal pad and the correspondent second metal pad.

8. The plurality of metal bumps of claim 1, wherein the space between two adjacent metal bumps that are sandwiched by the nonconducting substrate and the chip is filled with an anisotrpic conductive film (ACF).

9. The plurality of metal bumps of claim 1, wherein the insulating layer is made of silicon oxide or silicon nitride.

10. The plurality of metal bumps of claim 1, wherein the nonconducting substrate is a glass substrate.

11. A method of forming a plurality of metal bumps, comprising :

(a) providing a chip whose surface comprises a plurality of metal pads;

(b) forming a photoresist layer on the chip;

(c) performing an etching process to remove the photoresist layer covering the metal pad so as to form a hole that exposes the metal pad;

(d) filling the hole with a metal layer;

(e) completely removing the remaining photoresist layer;

(f) depositing an insulating layer on the chip to cover the metal layer; and

(g) performing an anisotropic dry etching process to remove the insulating layer positioned on the top of the metal layer and on the surface of the chip so as to leave the insulating layer positioned on the sidewall of the metal layer.

12. The method of claim 11, wherein the metal layer is made of Au.

13. The method of claim 11, wherein the insulating layer is made of silicon oxide or silicon nitride.

14. The method of claim 11, wherein the anisotropic dry etching process is a reactive ion etching (RIE) method.

15. The method of claim 11, wherein the metal bump is used for connecting the chip with a nonconducting substrate, and the space between two adjacent metal bumps is filled with an anisotropic conductive film (ACF).

16. A method of forming a plurality of metal bumps, comprising:

(a) providing a chip whose surface comprises a plurality of metal pads;

(b) forming a photoresist layer on the chip;

(c) performing a first etching process to removing the photoresist layer that covers the surface and periphery of the metal pad so as to form a first hole that exposes the metal pad;

(d) depositing an insulating layer on the chip to fill the first hole;

(e) performing a second etching process to remove the insulating layer positioned on the surface of the metal pad

and remain the insulating layer positioned on the sidewall of the first hole, and thereby a second hole is formed;

(f) filling the second hole with a metal layer; and

(g) removing the remaining photoresist layer.

17. The method of claim 16, wherein the metal layer is made of Au.

18. The method of claim 16, wherein the insulating layer is made of silicon oxide or silicon nitride.

19. The method of claim 16, wherein the metal bump is used for connecting the chip with a nonconducting substrate and the space between two adjacent metal bumps is filled with an anisotropic conductive film (ACF).